

AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): A semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power lines, the configuration comprising:

a semiconductor substrate;

an insulating layer disposed on the semiconductor substrate;

a power line disposed on the insulating layer; and

a plurality of interconnect structures disposed in the insulating layer with a first end on the substrate and in contact with the semiconductor substrate and a second end disposed substantially level with the power line therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate,

wherein the second end of the plurality of interconnect structures are disposed within a power line substantially enveloped by a dielectric layer in the power line, and

~~wherein the plurality of interconnect structures are substantially enveloped in an insulating layer.~~

2. (original): The semiconductor configuration of claim 1, further comprising a heat sink in contact with the substrate.

3. (original): The semiconductor configuration of claim 1, wherein each of the plurality of interconnect structures comprises at least one via stack.

4. (original): The semiconductor configuration of claim 3, wherein the plurality of interconnect structures are closed to the power line.

5. (original): The semiconductor configuration of claim 3, wherein at least one of the plurality of interconnect structures is joined to one other of the plurality of interconnect structures using a bridge structure.

6. (original): The semiconductor configuration of claim 3, including bridge structures, each of the bridge structures joins a respective one of the plurality of interconnect structures to one other of the plurality of interconnect structures.

7. (original): The semiconductor configuration of claim 3, wherein a width of each of the interconnect structures is from about 0.1 μ m to about 10 μ m.

8. (original): The semiconductor configuration of claim 3, wherein the interconnect structures are spaced apart from each other by a width of one of the interconnect structures.

9. (original): The semiconductor configuration of claim 3, wherein each of the plurality of bridges is alternatively spaced apart from a serpentine power line by a distance.

10. (original): The semiconductor configuration of claim 9, wherein the distance is a width of one of the plurality of interconnect structures.

11. (original): The semiconductor configuration of claim 3, wherein each of the plurality of interconnect structures is spaced apart from a linear power line by a distance.

12. (original): The semiconductor configuration of claim 11, wherein the distance is the width of one of the plurality of interconnect structures.

13. (cancelled)

14. (previously presented): The semiconductor configuration of claim 1, wherein the interconnect structures are alternatively spaced apart from each other by a width of one of the interconnect structures.

15. (previously presented): The semiconductor configuration of claim 1, wherein a ratio of the width of one of the interconnect structures to the power line is between about 1 to about 20.

16. (previously presented): The semiconductor configuration of claim 1, wherein a width of each of the interconnect structures is from about 0.1 μ m to about 10 μ m.

17. (previously presented): The semiconductor configuration of claim 1, wherein the interconnect structures are spaced apart from each other by a width of one of the interconnect structures.

18. (previously presented): The semiconductor configuration of claim 1, wherein each of the plurality of interconnect structures is alternatively spaced apart within the power line by a distance.

19. (previously presented): The semiconductor configuration of claim 18, wherein the distance is the width of one of the plurality of interconnect structures.

20. (previously presented): The semiconductor configuration of claim 1, wherein the power line has a serpentine shape.

21. (previously presented): The semiconductor configuration of claim 1, wherein the power line has a linear shape.

22-25. (cancelled)